

Running iVerilog

Jan 2014 - NOTE13: Running iVerilog... at school and home

Your design loop has three steps/programs: iverilog (compile), vvp (simulate), and gtkwave (graphically view results).

You can download iverilog (and vvp and gtkwave) here: www.bleyer.org/icarus

This is a useful link for getting started: iverilog.wikia.com/wiki/Getting_Started

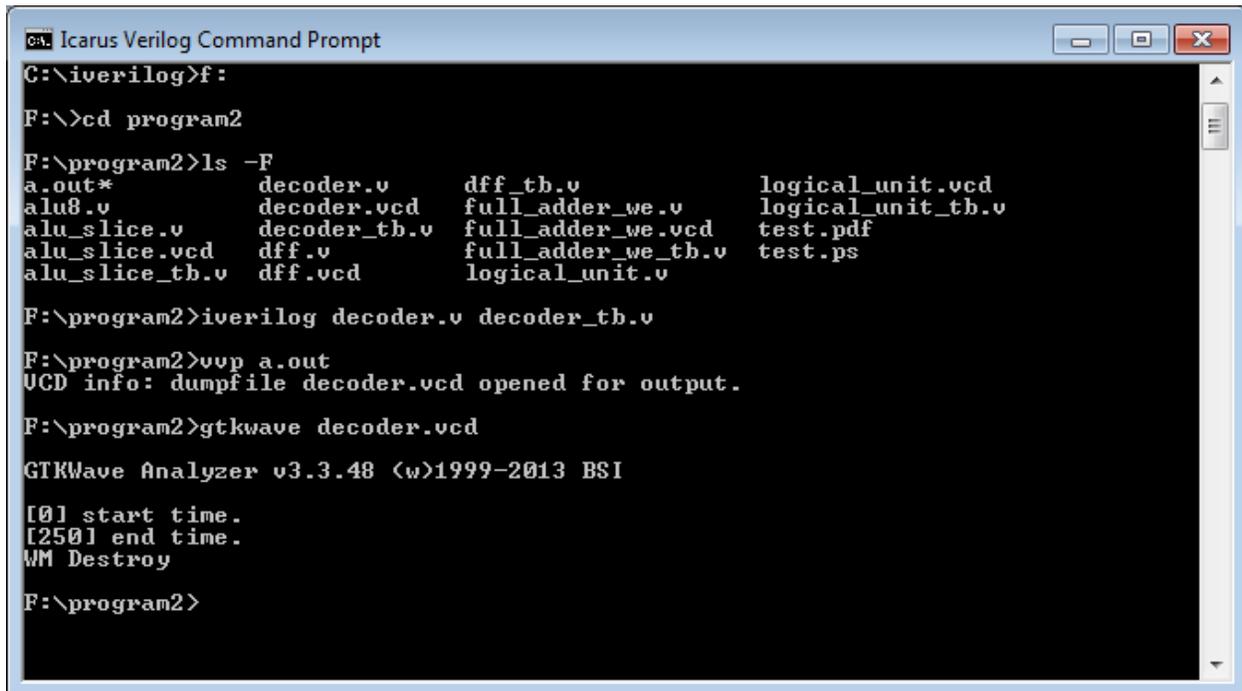
In the lab, ITS has a nice setup for using iVerilog:

- Select Start/Programs/Icarus Verilog/Icarus Verilog... this opens a Windows Explorer window at the iVerilog folder
- Double-click the "Use iverilog" script... this opens a black Command Prompt window (and makes sure your PATH variable is properly set)

About our three programs:

- `iverilog file1.v file2.v ...`
Compile your design. All files used in your design must be listed. If no errors, then the output is file `a.out`.
- `vvp a.out`
Simulate the design previously compiled in the `a.out` file. The output of this step is defined in your testbench. Our convention will be to name the output file `<mod>.vcd`, for example `decoder.vcd` in my example.
- `gtkwave file1.vcd`
Graphically view the input and output waveforms for your design.

Let's walk through an example... my decoder.



```
C:\Icarus Verilog>f:
F:\>cd program2
F:\program2>ls -F
a.out*          decoder.v      dff_tb.v      logical_unit.vcd
alu8.v          decoder.vcd    full_adder_we.v  logical_unit_tb.v
alu_slice.v     decoder_tb.v   full_adder_we.vcd test.pdf
alu_slice.vcd   dff.v         full_adder_we_tb.v test.ps
alu_slice_tb.v  dff.vcd       logical_unit.v

F:\program2>iverilog decoder.v decoder_tb.v

F:\program2>vvp a.out
UCD info: dumpfile decoder.vcd opened for output.

F:\program2>gtkwave decoder.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[250] end time.
WM Destroy

F:\program2>
```

Here's what's happening in the black window above (my typing is **bold**):

1. **f:** - set the current folder to my f: drive
2. **cd program2** - change directory to my program2 folder
3. **ls -F** - lists the contents of this folder (the -F is optional)
4. **iverilog decoder.v decoder_tb.v** - compile my Verilog design and testbench...
a.out file is created
5. **vvp a.out** - run the simulation... decoder.vcd file is created
6. **gtkwave decoder.vcd** - view the simulation results graphically

If everything works perfectly, then exit the window. Otherwise, keep this window. Make edits to your Verilog (I use Notepad++) and then do steps 4-6 over (and over) again.

Tip: in the Command Prompt window, use the arrow keys to scroll through previous commands you have typed. This can save you time and fingers.

Tip: <ALT>PrintScreen is how I grabbed that Command Prompt window. You can also use this to capture your graphical waveforms in gtkwave.