Mic-1 complete block diagram



Figure 4-6: Mic-1 complete block diagram (datapath + control)

Elements related to microcode execution:

- The **control store** is a ROM holding the microcode for Mic-1. ROM size is 512 words by 36 bits/word. 512 words requires 9 bits to address.
- A 4-to-16 Decoder is used to decode the 4 B bus bits and select a register to drive B.
- The MIR (Micro-Instruction Register) holds the current micro-instruction being executed.
- The MPC (Micro-Program Counter) holds the ROM address of the next micro-instruction.
- The **High bit** box determines the high bit of the next micro-instruction address using N, Z bits from the ALU and JAMN and JAMZ bits from the current micro-instruction.
- The O box below the MPC register is an OR gate. It OR's the Addr bits with PC if JMPC is true.

Determining the next micro-instruction:

- If JMPC is 0, then MPC set to the value of Addr. This Addr value is the "next address" field of the current micro-instruction being executed. Typically, this just increments the address to execute the next micro-instruction in a function, or it is a jump to a different part of the micro-program.
- If JMPC is 1, then MPC is set to the opcode stored in MBR. This means that a new opcode is loaded and we'll start executing micro-instructions from there. This also means that the opcode must be chosen to correspond to the ROM address of the micro-instructions that implement that opcode.
- When JMPC is 1, typically the value of Addr is 0x000 or 0x100 because that value is OR'd with the MBR address. In other words, the if a micro-instruction knows it's going to ask for the next opcode in MBR, then it will set its own "next address" to be 0.

Usually you can simplify things... JMPC=0 usually means execute the next micro-instruction of the current command. JMPC=1 usually means that a new IJVM command is starting.

Notice the dotted line around MAR, MDR, PC and MBR registers. These are the registers related to mem access.

The clock is not shown.